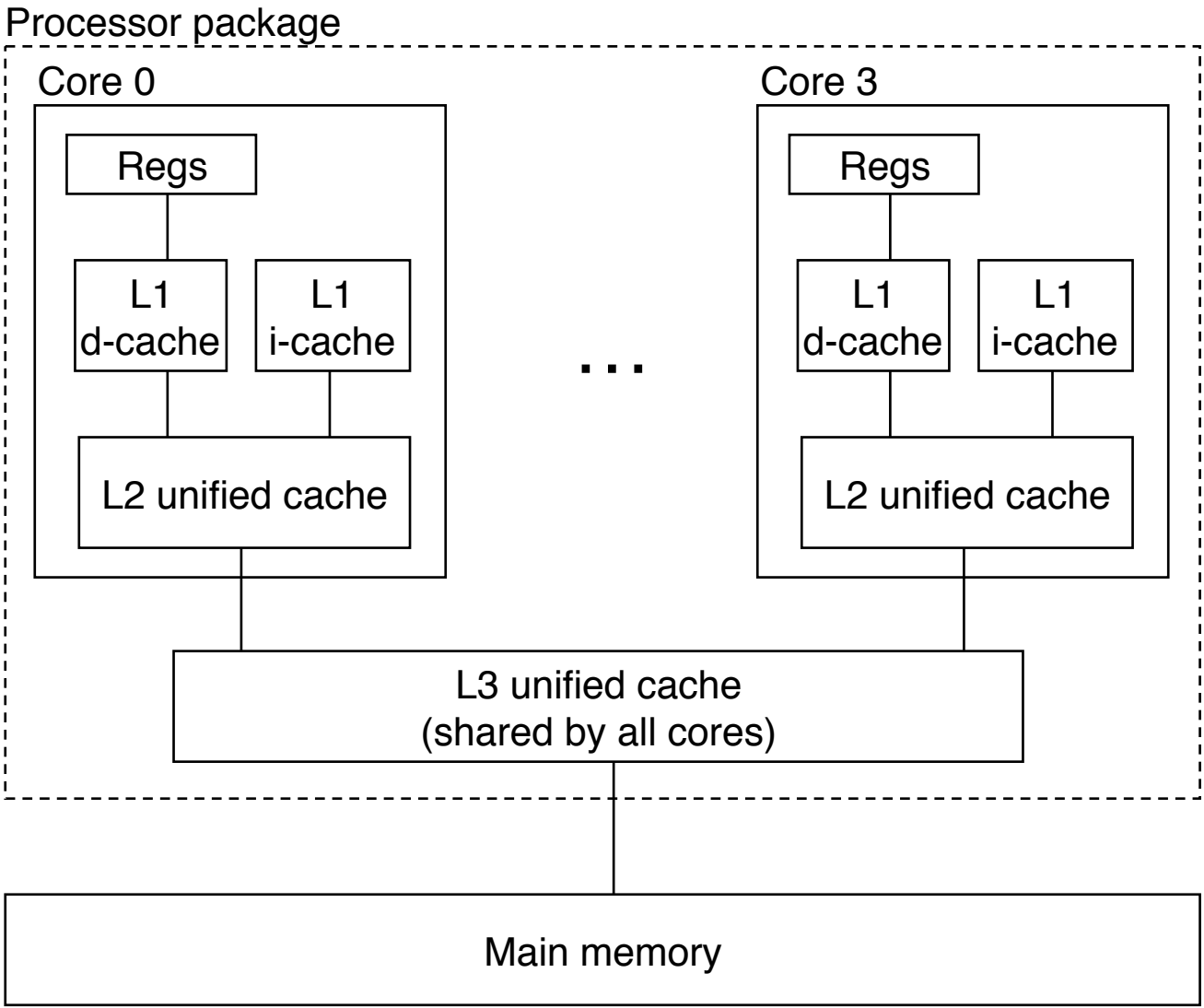
Processor package
Core 0
Regs
L1
d-cache
L1
i-cache
L2 unified cache
...
Core 3
Regs
L1
d-cache
L1
i-cache
L2 unified cache
L3 unified cache
(shared by all cores)
Main memory